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Low Noise Superjunction MOSFET with Integrated Snubber Structure

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***Abstract*— Novel superjunction (SJ)-MOSFET structure with distributed internal snubber area is proposed. RC network composed by gate electrode, oxide and P-type pillar provides frequency-dependent capacitive coupling between each terminal. The snubber area acts as gate-drain capacitance (C_{gd}) only at high-frequency band. Switching noise generated during turn-off transient is absorbed by the snubber without increasing switching loss. We verified the concept by simulation and experiments, and confirmed better trade-off between EMI (Electromagnetic interference) and efficiency.**

Keywords— superjunction; noise; switching loss

I. INTRODUCTION

High voltage MOSFETs are widely used in switching applications handling commercial power supply. Superjunction (SJ) is a main stream structure for 300-900V voltage ratings achieving superior specific on-resistance ($R_{on}A$) lower than Si-limit [1]. Compared to advanced compound semiconductor devices such as GaN HEMT and SiC MOSFET, SJ-MOSFET is easy to handle for designers using conventional MOSFETs in terms of noise controllability. Therefore the improvement of the performance has still been demanded. The $R_{on}A$ of SJ-MOSFET has been improved by pitch shrinking and optimization of doping profile of SJ structure which enable reduction of conduction and switching loss [2]-[4]. However, advanced SJ-MOSFETs are sometimes difficult to use because of their high speed switching characteristics. In order to control the switching speed, several techniques are proposed; mesh gate structure to keep gate-drain capacitance (C_{gd}) large [5] or controlling switching speed by optimizing internal gate resistance [6]. However, these strategies increase switching loss by reducing switching speed. Breakthrough of the trade-off between the switching noise and loss further accelerates the application field of SJ-MOSFETs.

In this report, novel SJ-MOSFET with internal snubber is presented. With this structure, switching noise is effectively suppressed by increasing C_{gd} only at high-frequency operation. The trade-off between radiated noise level and efficiency is improved.

II. SWITCHING NOISE GENERATION MECHANISM

The process of switching noise generation can be explained by analyzing small signal equivalent circuit. Fig.1 shows turn-off transient simulation waveform of inductive load switching by SJ-MOSFET in case of parasitic inductances in the circuit. After gate-source voltage (V_{gs}) falls below gate plateau voltage, the channel current (I_{ch}) starts to drop. The drop-off of I_{ch} is compensated by displacement current (I_{cds} and I_{cgd}) generated by discharging C_{ds} and C_{gd} in order to keep the inductive load current constant. The interval of this process, so-called "miller interval", highly depends on C_{gd} characteristic controlling the switching speed. After C_{ds} is discharged, C_{ds} rapidly decreases by the depletion of SJ. Then V_{ds} starts to rise and I_{cds} falls sharply, because the displacement current ($C_{ds}*dV_{ds}/dt$), also becomes small. Affected by the decrease of I_{cds}, source current (I_s) suddenly drops, and the high dI_s/dt generates voltage drop by parasitic inductance at the end of the miller interval. As a result, source voltage falls down and the gate voltage is also lowered by capacitive coupling via C_{gs}. These fast transients will be the cause of EMI or self turn-on of the MOSFET, resulting noisy switching behavior with low efficiency. Particularly high-frequency noise (e.g. >100MHz) is difficult to suppress by the circuit design, because even package leads (~10nH) become large parasitic impedance at high-frequency band and modification of the layout is not always effective.

Therefore reduction of noisy transients by the device itself is essential for next generation SJ-MOSFETs with ease of use. Especially C_{gd} behavior during miller interval at turn-off process should be designed carefully, while considering the effect on switching loss.

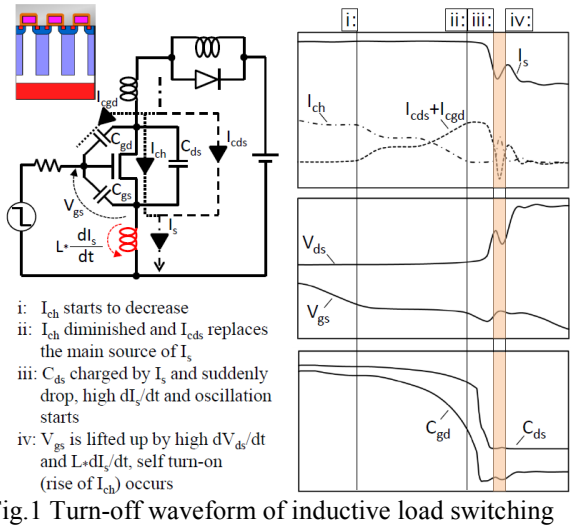

Fig.1 Turn-off waveform of inductive load switching simulation by SJ-MOSFET with parasitic inductances. Static capacitance curves (C_{gd}, C_{ds}) estimated from V_{ds} are also shown.

III. STRUCTURE, MECHANISM AND SIMULATIONS

To manage both noise characteristic and switching loss, we developed a device having C_{gd} characteristic depending on the operation condition. Fig.2 illustrates the proposed structure composed by conventional MOSFET (Cut plane A) and snubber area (Cut plane B). In the conventional MOSFET area, gate oxide and electrode are only formed on each N-pillar. In the snubber region, the gate structures are also formed on alternate P-pillars. These P-pillars are connected to source electrode through the pillars themselves and base region in the conventional area along the pillar stripe direction. No additional process step is required since the snubber is composed by fundamental SJ and MOS structures.

The effect of the snubber area is explained by an equivalent circuit described by RC network connected to the conventional cell region (Fig.3). The additional area is composed by gate electrode, resistance of P-pillar (R_{sp}), oxide capacitance between gate electrode and P/N-pillar (C_{gp}/C_{gn}), and SJ pillar capacitance (C_{pn}). By the existence of R_{sp} in the circuit, electronic coupling between each electrode depends on signal frequency and V_{ds}. At low frequency, the gate potential mainly couples to source potential through C_{gp} and R_{sp}, because the impedance of R_{sp} is smaller than C_{pn} ($R_{sp}<<1/2\pi fC_{pn}$). On the other hand, the gate electrode couples to drain electrode via C_{gp} and C_{pn} at high frequency. Namely, effective gate-drain capacitance is increased by the additional capacitance of the snubber area. The frequency, at which the snubber acts as added C_{gd}, can be controlled with R_{sp} by changing snubber layout. Therefore, C_{gd} can be increased at only high-frequency band (e.g. >100MHz), while keeping C_{gd} and switching loss small at switching frequency (e.g. ~100kHz). Furthermore, the snubber effect is enhanced at the turn-off timing of V_{ds} rise. P-pillar is depleted as V_{ds} increases, then R_{sp}, resistance composed by the P-pillar, becomes large by the extraction of holes in the pillar (Fig.4(a)). The increase of R_{sp} accelerates the coupling between gate and drain potentials. As Fig.4(b) indicates, C_{gd}-V_{ds} curve with the snubber structure has clear frequency dependence. The effect of the snubber on switching characteristic is evaluated by simulation (Fig.5). By modifying the capacitance curve by the snubber, switching noise is effectively suppressed. In addition, self turn-on behavior is also suppressed, which will contribute to the improvement of the set efficiency.

Consequently, the snubber acts as added C_{gd} only at noise-concerned frequency. The proposed structure will realize low switching loss and noise level at the same time.

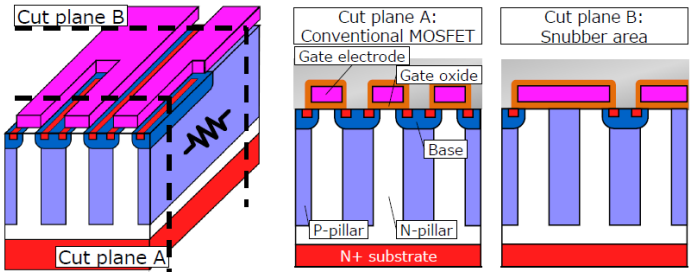

Fig.2 Proposed SJ MOSFET structure with internal snubber.

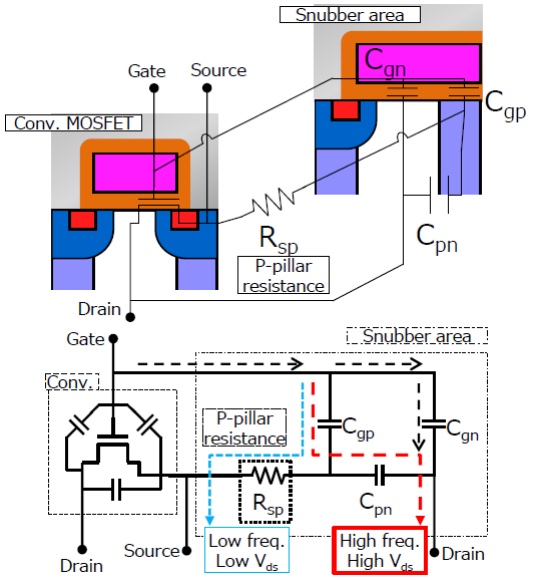

Fig.3 Equivalent small signal circuit of the proposed structure and schematic signal flow dependence on frequency and V_{ds}.

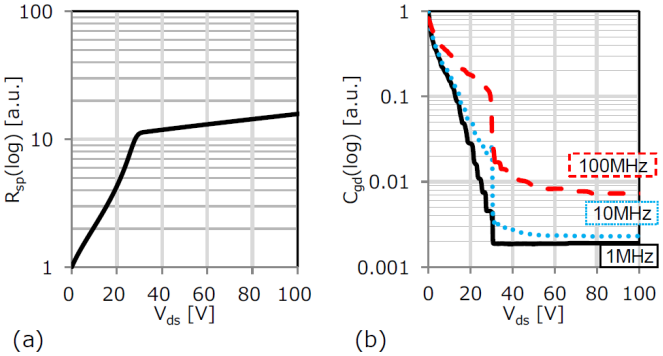

Fig.4 Simulated R_{sp}-V_{ds} and C_{gd}-V_{ds} curve of the proposed structure.

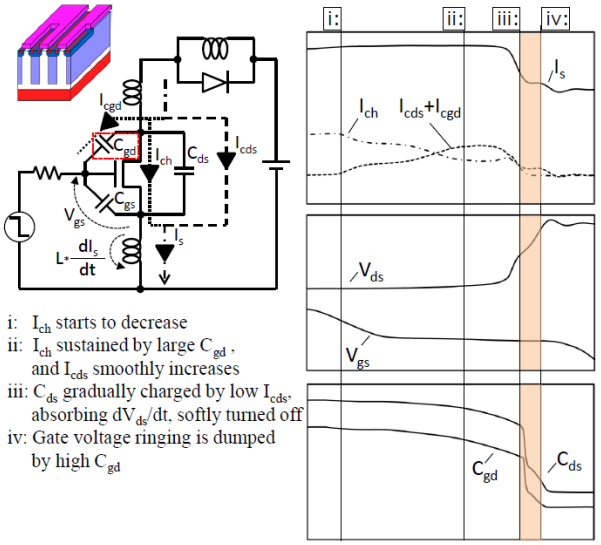

Fig.5 Inductive load switching simulation waveform of the proposed structure with static capacitance curves at 100MHz.

IV. EXPERIMENTS

We fabricated test samples and evaluated static and dynamic characteristics. Three gate layouts are considered: stripe, mesh and snubber. Fig.6 shows schematic figures of each structure. Voltage and current ratings are 600V/12A. Each device is on the same wafer and only the plane layout is changed. Samples are assembled with TO-220FP package.

Table.1 summarizes DC characteristics for each structure normalized by the result of the stripe structure. The main differences between each structure are $R_{on}A$ and V_{th}, resulting from the difference in channel width indicated in the table. Focusing on the capacitive behavior, C_{gd} and gate charge (Q_g) characteristics are evaluated. Fig.7 shows the C_{gd}-V_{ds} curve at low frequency regime (100kHz). Stripe structure has the smallest capacitance because of small gate electrode area. Mesh and snubber samples having similar gate area show almost the same C_{gd} curve at all V_{ds} range. Reflecting the differences of C_{gd}, Q_g characteristic has structure dependence (Fig.8). Same as C_{gd}, stripe has smallest Q_{gd}, and mesh and snubber have almost the same Q_{gd}. Note that Q_g measurement is conducted at quite slow switching of a few tens of microseconds, which is relatively slow compared to the actual usage at switching mode power supply.

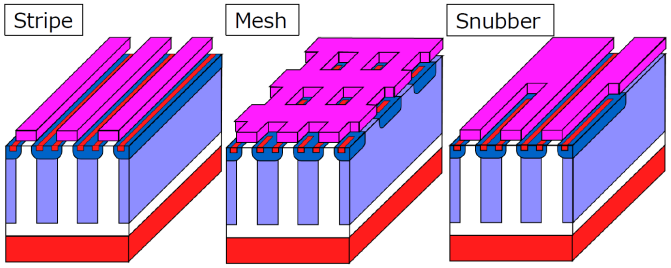

Fig.6 Gate layout structure of fabricated samples.

Table.1 DC characteristics

Gate layout	Channel width	Gate electrode area	BV	$R_{on}A$	Vth
Stripe	100%	100%	100%	100%	100%
Mesh	30%	156%	101%	109%	113%
Snubber	51%	158%	101%	108%	112%

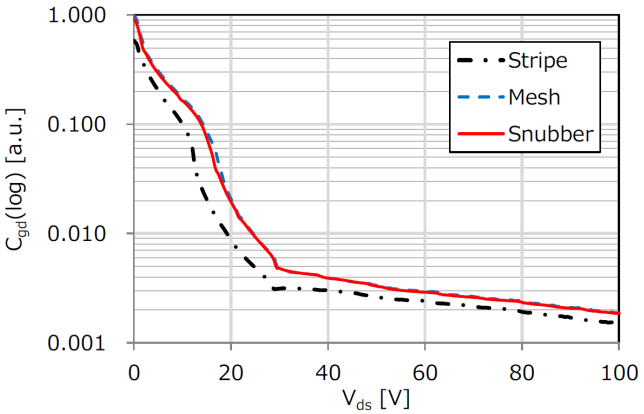

Fig.7 C_{gd} -V_{ds} curves of each structure at 100kHz.

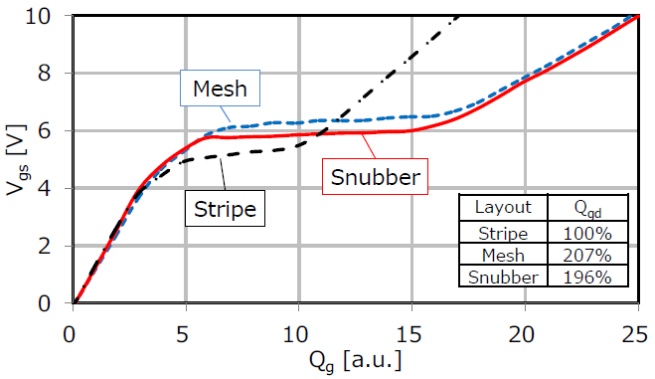

Fig.8 Gate charging characteristics (V_{gs} -Q_g).

In slow transient tests described above, the proposed structure shows almost the same characteristic as mesh structure. By contrast, the snubber structure effectively suppresses the noise at actual switching operation. Fig.9 illustrates inductive load turn-off switching waveforms of each sample at almost equivalent turn-off loss. As predicted from small C_{gd} and Q_{gd}, stripe has the fastest and noisy switching characteristic (Fig.9(a)). On the other hand, snubber device (Fig.9(c)) shows small switching noise compared to mesh sample having almost the same C_{gd} and Q_{gd} (Fig.9(b)). Especially, gate voltage oscillation is effectively suppressed. The oscillation frequency is around 130 MHz which is high enough for activating the snubber effect of increasing C_{gd}. Owing to the added C_{gd} in high-frequency band, smooth switching is achieved with the proposed structure.

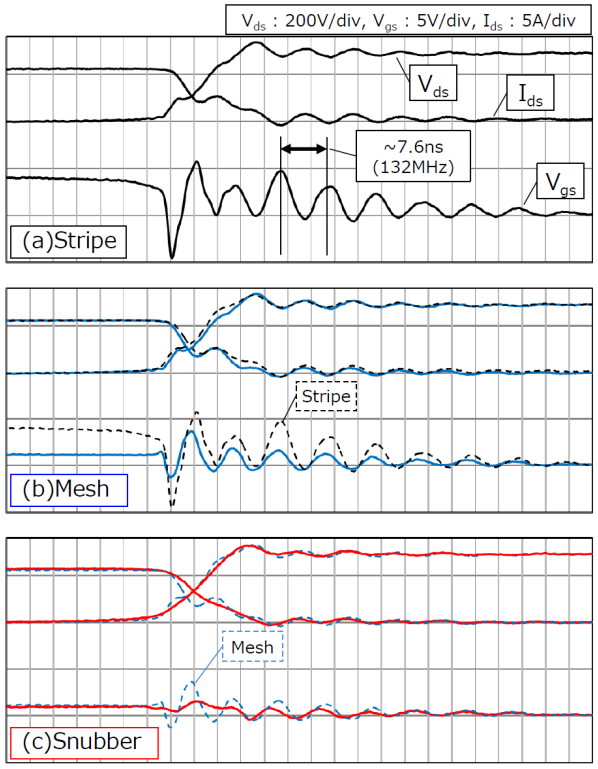

Fig.9 Inductive load turn-off waveform of each structure.

Dotted lines are for comparison among samples.

For the purpose of clarifying the improvement in actual usage, the devices are tested in power factor collection (PFC) circuit of AC-DC converter with output of 200W (Fig.10). Efficiency and radiated noise emission at full load condition are evaluated. The switching speed was varied by changing gate drive resistance in order to investigate the trade-off between the efficiency and noise level.

Fig.11 shows radiated noise spectrum of each device. The noise level is reduced by the adoption of the snubber structure at the entire frequency band. Especially, the peak level around 200MHz and 400MHz are clearly suppressed with the proposed structure. The relationship between efficiency and the maximum noise level is shown in Fig.12. As external gate resistance (R_g) is increased, the switching speed is slowing down, having trade-off between these characteristics. The proposed snubber structure shows better trade-off compared to conventional stripe and mesh devices. That is, reduction of radiation noise level is expected at targeting efficiency.

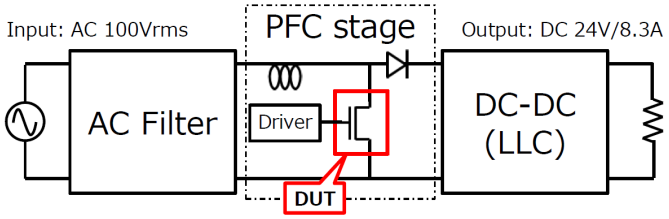

Fig.10 Schematic circuit of AC-DC converter.

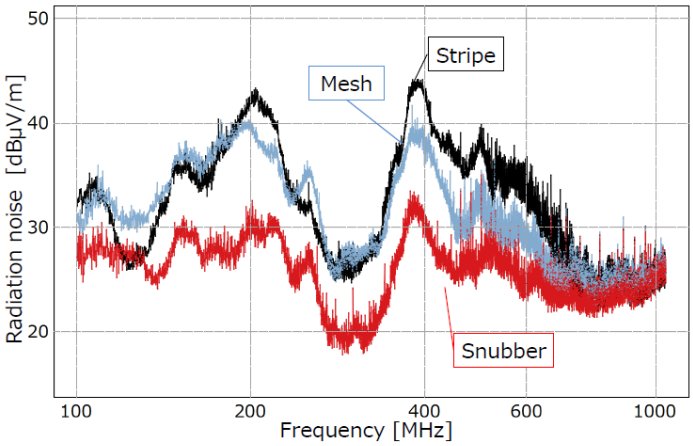

Fig.11 Noise spectrum of each gate layout. Efficiency is fixed at almost the same level (90.4~90.5%) by modifying external gate resistance of the gate driver.

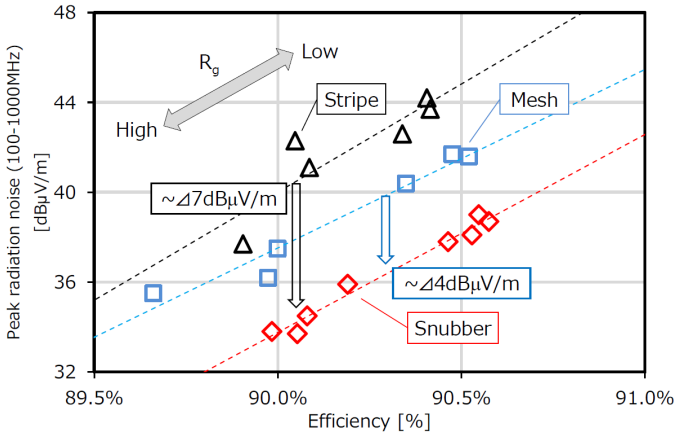

Fig.12 Relationship between radiated noise and efficiency.

V. Conclusion

The novel SJ-MOSFET structure with internal snubber is proposed. By adding the snubber area, effective gate-drain capacitance is modulated and increased at high-frequency, resulting in EMI noise suppression. High efficiency with low noise emission level is achieved.

Acknowledgment

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