K. Mori et al., “3D Packaging and Integration Technology using Photosensitive Mold”, Extended Abstracts of the 2020 International Conference on Solid State Devices and Materials (SSDM), Virtual conference, 2020, pp131-132
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3D Packaging and Integration Technology using Photosensitive Mold

Kentaro Mori, Soichi Yamashita and Masahiro Sekiguchi

Toshiba Electronic Devices and Storage Corporation
33, Shinisogo-Cho, Isogo-ku, Yokohama 235-0017, Japan
Phone: +81-45-759-1600 E-mail: kentaro3.mori@toshiba.co.jp

Abstract

3D packaging and integration using photosensitive mold is promising technology to reduce costs and improve productivity for future heterogeneous integration. By applying a mold material with characteristics such as photo via opening, low viscosity, filler-less, thick and film shape to fan-out package, an innovative 3D integration with high design flexibility can be expected. We have confirmed the feasibility of the 3D integration packaging process, and evaluated the package reliability assessment for photo vias with different diameters and depths. The developed package has been evaluated by thermal cycle test (TCT). After a 1000-cycle TCT, electron backscatter diffraction (EBSD) analysis was adopted to analyze the thermal stress on the Cu Redistribution Layer (RDL). The developed package using photosensitive mold showed high reliability and the possibility of applying it as future 3D package for integration was confirmed.

1. Introduction

Fan-out wafer-level packaging (FOWLP) is a mainstream technology for 3D packaging and integration. Current 3D fan-out package technology based on Package-on-Package (PoP) has already realized high-density interconnections between logic and memory devices in mobile applications. Its PoP-based packages using epoxy molding compound (EMC) usually require tall electroplated Cu pillars after thick photoresist patterning process. The top surface of the Cu pillars has to be exposed by chemical mechanical polishing (CMP) of the mold surface to interconnect the two packages [1-2]. The thick photoresist and CMP processes required to form tall Cu pillars are costly. Therefore, various methods for lowering costs and increasing density for through-mold interconnects have been developed [3-5]. We developed 3D packaging and integration based on fan-out technology using a photosensitive mold material to reduce costs and improve productivity compared with conventional EMC [6]. Simplified process flow, high-density photo via, and reliability assessment were demonstrated in this paper.

2. Fabrication

Si test dies, with 10 mm x 10 mm size and 100 μm thickness as shown in Table I, were prepared to confirm feasibility and evaluate the reliability test of the 3D integration package. Figure 1 shows the fabrication process for the package with photosensitive mold. Firstly, the die was mounted face up on 8 inch Si substrate (Fig. 1(a)) and embedded in a more than 100 μm-thick low-viscosity photosensitive mold film by means of a vacuum lamination process (Fig. 1(b, c)). After curing the film to realize a thickness of 110 μm, the lithography process was executed to form openings in the film with depth of 10 μm on the Al pads of the embedded chip as shallow vias, and with depth of 110 μm on the Cu pads of the substrate as deep vias (Fig. 1(d)). The two lithography process options are available to form vias with different depths and sizes. One is a multiple exposure process for different depth vias using different designed photo-masks for each type of vias described in Fig. 2(a). In the other process, all via openings are formed by a single exposure using one mask with the exposure condition targeting the deepest via opening described in Fig. 2(b). In this study, the mask diameter for shallow vias is 60 μm and that for deep vias is 100 μm. 400 mJ/cm2 was adopted as the exposure condition for forming shallow vias. It was confirmed that the shrinkage from the mask diameter was 6 μm. Similarly, 1600 mJ/cm2 was adopted as the exposure condition for forming deep vias. It was confirmed that the shrinkage from the mask diameter was 20 μm (Fig. 2(a)). In contrast, even if the exposure amount for shallow vias is the same as for deep vias (1600 mJ/cm2), shallow vias can be formed with a larger shrinkage amount (27 μm) (Fig. 2(b)). The one-time process is a cost-effective solution for greater productivity improvement. Cu RDLs were fabricated to connect Al bond pads on the die with Cu pads on the substrate in the usual manner using Cu/Ti sputtering deposition, resist patterning, Cu electroplating, photoresist removal, and etching of sputter-deposited Cu and Ti (Fig. 1(e)). In the final step, the thin photosensitive mold was coated on the whole substrate as a top solder resist (Fig. 1(f)).

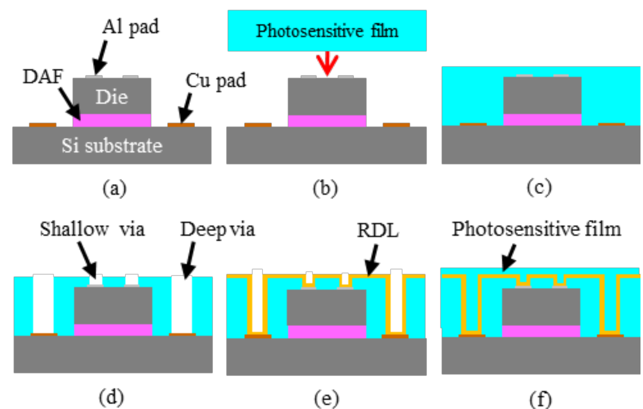

Fig. 1 Fabrication process with photosensitive mold. (a) Die mounting on Si wafer using die attach film (DAF). (b-c) Thick photosensitive mold film lamination. (d) Via opening. (e) Metallization layer formation. (f) Thin photosensitive mold film lamination.

Table I Die specification

Size (mm)	10 x 10
Thickness (μm)	100 (including DAF)
Pad pitch (μm)	200
Pad count	2,116

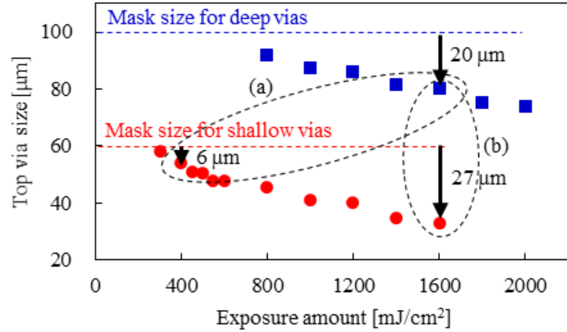

Fig. 2 Relation between the exposure dose and via top diameter. (a) multiple exposure process, (b) one-time process.

3. Results and Discussion

Figure 3 shows a photograph of the embedded die edge. There is no significant step gap at the edge of the die. A die is embedded face-up in the photosensitive mold. RDL interconnects the deep via on the substrate with the shallow via on the embedded die. The gap in this process is less than 3 μm. The void-free gap filling and flat surface are confirmed after film formation. And formation of the deep via openings with height of 110 μm, top diameter of 80 μm, and aspect ratio of 1.4 is confirmed. The deep vias can be placed with a 150 μm pitch. Compared with the conventional Cu pillar process, the 3D integration can provide higher pin counts.

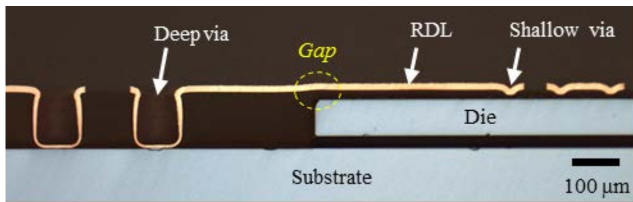

Fig. 3 Cross sections of the embedded die edge.

Reliability assessment of the packaged samples was performed. Daisy chains connecting over 2000 vias with 200 μm pitch on the die and over 700 vias with 300 μm pitch on the substrate were checked to measure their electrical resistance. Before the test, all package samples are rated at a moisture sensitivity level-3 conditions (MSL 3). 1000-cycle package-level TCT (-55 degC/125 degC) confirmed that tiny cracks occurred at the top edge of the via openings in Fig.4 (c). EBSD was employed to characterize the orientation of grains, grain size distribution, and strain mappings of the Cu films before and after 1000 thermal cycles. Residual stress around the crack was confirmed from grain reference orientation deviation (GROD) in Fig.4 (d). It was also revealed that the grain size after the 1000 thermal cycles was enlarged compared with that before the thermal cycling, which causes tiny cracks along the grain boundaries. However, the failure criterion was higher than 10% shift of the electrical resistance of the daisy chain in this work. The developed package with the photosensitive mold has no failures after 1000-cycle TCT as shown in Fig. 5.

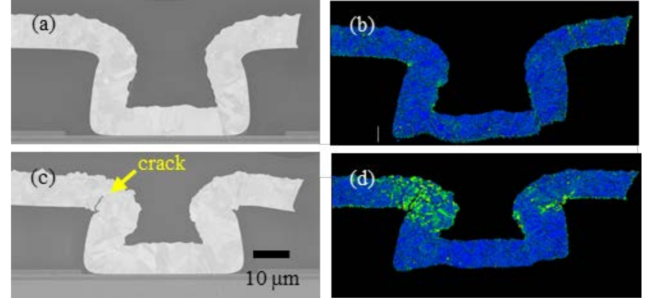

Fig. 4 SEM image and GROD maps of shallow via. (a, b) initial, (c, d) after 1000 thermal cycles.

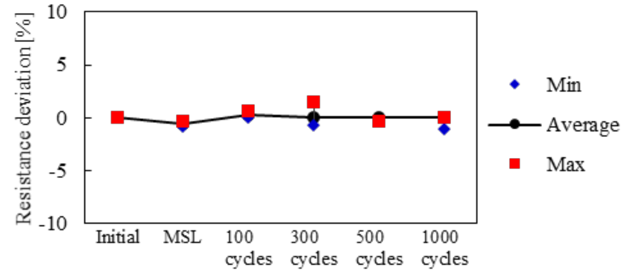

Fig. 5 Resistance deviation during thermal cycle test.

4. Conclusions

An innovative 3D packaging and integration technology with photosensitive mold was presented. After a test die was embedded in a thick photosensitive mold film, the lithography process conditions for shallow via on the die and deep via around the die were well optimized to realize a 3D integration package. The developed package with photosensitive mold passed a 1000-cycle thermal cycle test. This study revealed future viability of a fan-out process using a photosensitive mold to enhance 3D integration capability, thereby realizing a dramatic expansion of the application field for fan-out packages.

Acknowledgements

This study is based on results obtained from a project commissioned by the New Energy and Industrial Technology Development Organization (NEDO) to develop cross-sectoral technologies for IoT promotion. The authors thank Mr. S. Akejima and Dr. H. Ezawa for their encouragement and useful discussions on this research.

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