1 kW Full-Bridge DC-DC Converter Operation Guide

RD170-OGUIDE-01

TOSHIBA ELECTRONIC DEVICES & STORAGE CORPORATION

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1. Introduction

This operation guide describes operation of phase-shifted full-bridge topology which is used for the 1 kW full-bridge DC-DC converter (this power supply). Refer to the Reference Guide for the specifications, operating procedure, and performance of this power supply, and to the Design Guide for the circuit design of this power supply.

2. Phase-Shifted Full-Bridge (PSFB) DC-DC Converter Circuit

Fig. 2.1 shows the phase-shifted full-bridge (PSFB) DC-DC converter circuit. Q_1 to Q_8 in Fig. 2.1 shows MOSFET and D_{Q1} to D_{Q8} shows MOSFET body diode. In addition, C_{Q1} to C_{Q8} indicates the parasitic capacitance of MOSFET and L_r indicates the leakage inductance of the transformer TR.

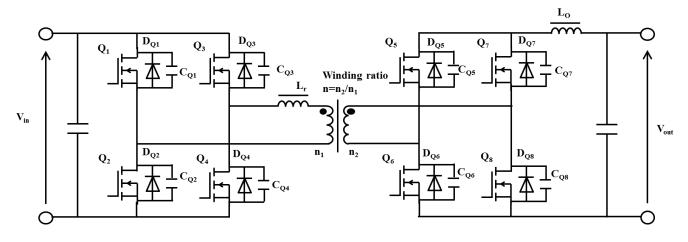


Fig. 2.1 Operation Description Circuit

3. Operation Signal and Output Waveform

Fig. 3.1 shows an example of the input gate signal waveform for each MOSFET and the output voltage and current waveforms for the primary and secondary sides. The waveform is only an image, and the dead time for switching between the upper and lower MOSFET is shown longer than the actual value.

The primary Q_1 and Q_2 are switched at -50 % duty and 180 degrees out of phase with each other. Q_3 and Q_4 are also switched similarly. Q_3 and Q_4 switching signals are phase-shifted relative to Q_1 and Q_2 switching signals. This phase shift determines the amount of overlap in the diagonally located MOSFETs and also determines the amount of energy transferred during this overlap period. The secondary side is a circuit that rectifies the energy transmitted from the primary side.

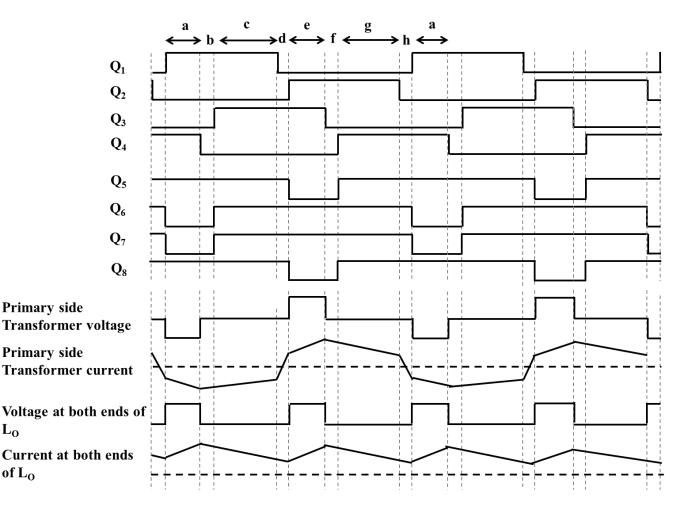


Fig. 3.1 Input Signal and Output Voltage, Current Waveform

3.1. Operation Signal and Output Waveform

This section explains the circuit operation in each period of a to h shown in Fig. 3.1.

Period a : Power Transfer to the Secondary Side

[Primary Side] Q_1 and Q_4 are On

The period during which power is transferred from the primary side to the secondary side through the transformer TR. In this case, the primary winding voltage is the input voltage (V_{in}).

Input voltage V_{in} is applied to the primary side of the transformer TR in the negative direction.

[Secondary Side] Q_5 and Q_8 are On

Voltage n x V_{in} corresponding to the winding ratio is applied to the secondary winding. The current in the secondary winding flows from the source to drain of Q_5 , then from L_o , and then returns to the secondary winding after flowing from source to drain of Q_8 . During this period the power is supplied to the secondary side.

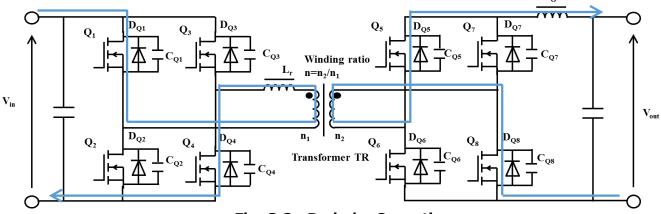


Fig. 3.2 Period a Operation

Period b-1 : C_{Q3}, C_{Q4} Charge/Discharge

[Primary Side] Only Q1 is On

After Q_4 turns off, C_{Q4} is charged in the following way:

 V_{in} Positive side $\rightarrow Q_1 \rightarrow n_1$ Winding $\rightarrow L_r \rightarrow C_{Q4} \rightarrow V_{in}$ Negative side

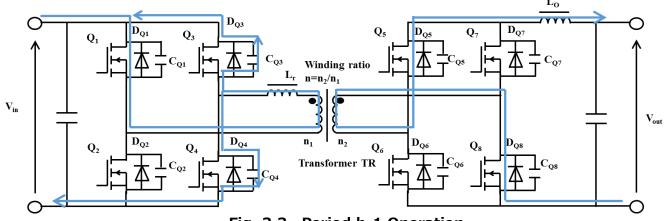
The moment when Q_4 turns off, the voltage across C_{Q4} is 0V, thus Q_4 turn off becomes ZVS. While C_{Q4} is getting charged, C_{Q3} is discharged in the following way:

 $C_{Q3}\!\rightarrow Q_1\!\rightarrow n_1$ Winding $\rightarrow L_r \rightarrow C_{Q3}$

After C_{Q3} and C_{Q4} have been charged/discharged, the unit proceeds to the next operation.

[Secondary Side] Q₅ and Q₈ are On

Operation of period a continues.





Period b-2 : D_{Q3} Conduction

[Primary Side] Only Q₁ is On

The energy accumulated in L_r continues to flow through the following path even after C_{Q3} and C_{Q4} have been charged/discharged.

 $L_r \rightarrow D_{Q3} \rightarrow Q_1 \rightarrow n_1 \text{ Winding} \rightarrow L_r$

In this condition, Q_3 turns on and system moves to the next operation. At this time, since D_{Q3} is conducting, the Q_3 voltage is approximately 0 V and thus Q_3 turn on is ZVS.

[Secondary Side] Q_5 and Q_8 are On

Operation of period a continues.

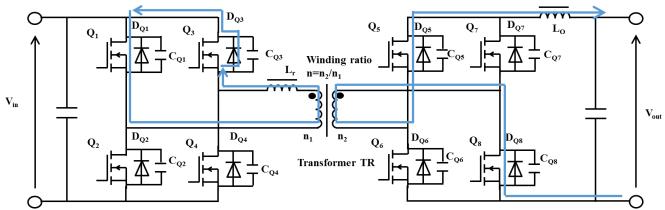


Fig. 3.4 Period b-2 Operation

<u>Period c : Q₃ Conduction (Continuation of current flow through inductor)</u> [Primary Side] Q₁ and Q₃ are On

After Q_3 turns on, current continues to flow through the following paths because of L_r energy:

 $L_r \rightarrow Q_3 \rightarrow Q_1 \rightarrow n_1 \text{ Winding} \rightarrow L_r$

The current of L_r gradually decreases, and the energy accumulated in L_r gradually decreases. [Secondary Side] Q_5 , Q_8 , Q_6 , and Q_7 are On

On secondary side, in addition to Q_5 and Q_8 , Q_6 and Q_7 are also turned on. Therefore, current flows through following two paths; first is from the source to drain of $Q_8 \rightarrow n_2$ Winding \rightarrow source to drain of Q_5 , and second is from the drain to source of $Q_7 \rightarrow n_2$ Winding \rightarrow drain to source of Q_6 .

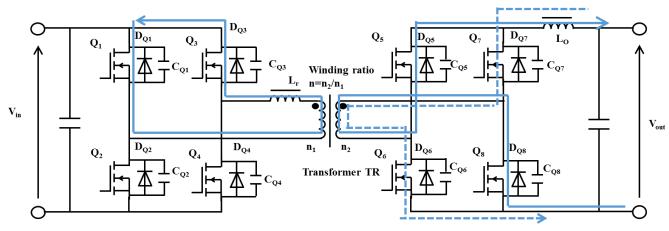


Fig. 3.5 Period c Operation

Period d-1 : C_{Q1}, C_{Q2} Charge/Discharge

[Primary Side] Only Q_3 is On

Even after Q_1 turns off, current continues to flow through the following paths because of L_r energy:

 $L_r \rightarrow Q_3 \rightarrow C_{Q1} \rightarrow n_1 \text{ Winding} \rightarrow L_r$

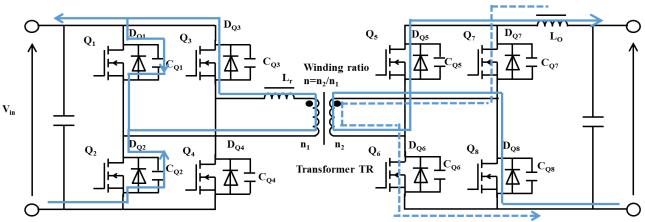
While C_{Q1} is getting charged, C_{Q2} is discharged in the following way:

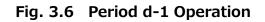
 $L_r \rightarrow Q_3 \rightarrow V_{in} \rightarrow C_{Q2} \rightarrow n_1 \text{ Winding} \rightarrow L_r$

When charging/discharging of C_{Q1} and C_{Q2} is completed, the system moves to next operation.

[Secondary Side] Q_5 , Q_8 , Q_6 , and Q_7 are On

Operation of period c continues.





Period d-2 : D_{Q2} Conduction

[Primary Side] Only Q₃ is On

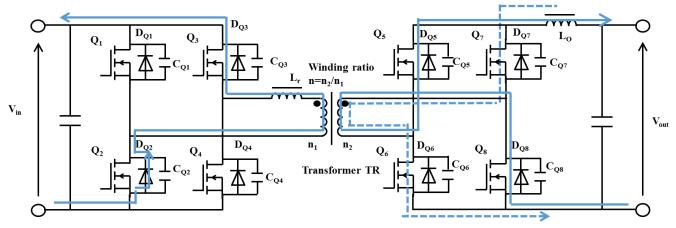
The energy accumulated in L_r continues to flow through the following path even after C_{Q1} and C_{Q2} have been charged/discharged.

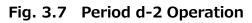
 $L_r \rightarrow Q_3 \rightarrow V_{in} \rightarrow D_{Q2} \rightarrow n1 \text{ Winding} \rightarrow L_r$

In this condition, Q_2 turns on and the system moves to next operation. Because D_{Q2} is conducting, Q_2 voltage is approximately 0 V and thus Q_2 turn on is ZVS.

[Secondary Side] Q₅, Q₈, Q₆, and Q₇ are On

Operation of period c continues.





Period d-3 : Q₂ Conduction

[Primary Side] Q_2 and Q_3 are On

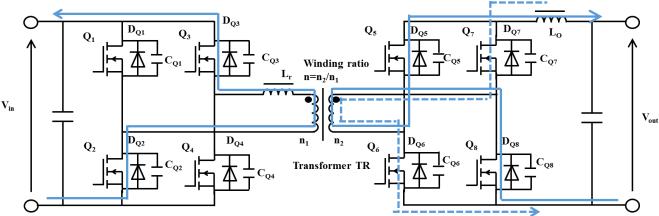
After Q₂ turns on, current continues to flow through the following paths because of L_r energy:

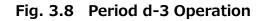
 $L_r \rightarrow Q_3 \rightarrow V_{in} \rightarrow Q_2 \rightarrow n_1 \text{ Winding} \rightarrow L_r$

In L_r , the incoming voltage V_{in} is applied in the direction that opposes this current flow, and thus the current of L_r is rapidly reduced, and is immediately inverted, and then the system moves to the next operation.

[Secondary Side] Q₅, Q₈, Q₆, and Q₇ are On

Operation of period c continues.





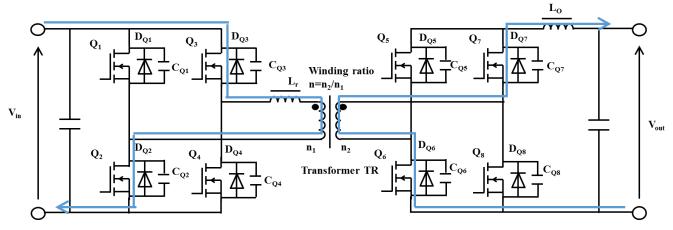
Period e : Power Transfer to the Secondary Side

[Primary Side] Q₂ and Q₃ are On

This is the period during which power is transferred from the primary side to the secondary side through the transformer TR. In this case, the primary winding voltage is the input voltage (V_{in}).

[Secondary Side] Q_6 and Q_7 are On

Voltage n x V_{in} corresponding to the winding ratio is applied to the secondary winding. The current in the secondary winding flows from the source to drain of Q_7 , then from L_0 , and then returns to the secondary winding after flowing from the source to drain of Q_6 . This is the period during which power is supplied to the secondary side.





Period f-1 : C_{Q3}, C_{Q4} Charge/Discharge

[Primary Side] Only Q_2 is On

After Q_3 turns off, C_{Q3} is charged in the following way:

 V_{in} Positive side $\rightarrow C_{Q3} \rightarrow L_r \rightarrow n_1$ Winding $\rightarrow Q_2 \rightarrow V_{in}$ Negative side

When Q_3 turns off, C_{Q3} voltage is 0V, so Q_3 turns off to ZVS.

While C_{Q3} is getting charged, C_{Q4} is discharged in the following way:

 $C_{Q4} {\rightarrow} L_r {\rightarrow} n_1 \text{ Winding} {\rightarrow} Q_2 {\rightarrow} C_{Q4}$

After C_{Q3} and C_{Q4} have been charged/discharged, the system moves to the next operation.

[Secondary Side] Q_6 and Q_7 are On

Operation of period e continues.

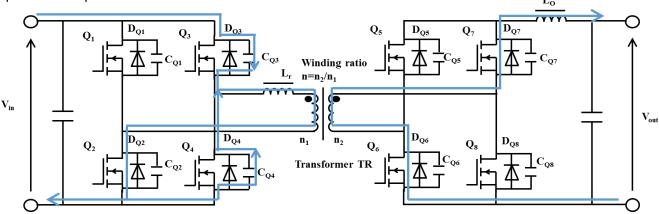


Fig. 3.10 Period f-1 Operation

Period f-2 : D_{Q4} Conduction

[Primary Side] Only Q_2 is On

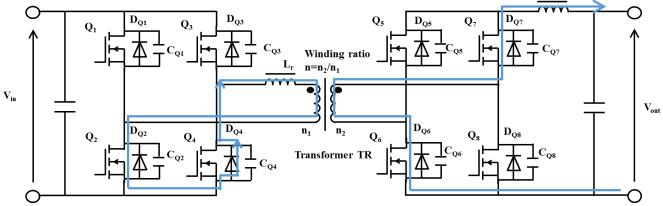
The energy accumulated in L_r continues to flow through the following path even after C_{Q3} and C_{Q4} have been charged/discharged.

 $L_r \rightarrow n_1 \text{ Winding} \rightarrow Q_2 \rightarrow D_{Q4} \rightarrow L_r$

In this condition, Q_4 turns on and the system moves to the next operation. At this time, since D_{Q4} is conducting, Q_4 voltage is approximately 0 V and thus Q_4 turn on is ZVS.

[Secondary Side] Q_6 and Q_7 are On

Operation of period e continues.





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Period g : : Q₄ Conduction (Continuation of current flow through inductor)

[Primary Side] Q_2 and Q_4 are On

After Q_4 turns on, the energy accumulated in L_r continues to flow through the following path.

 $L_r \rightarrow n_1 \text{ Winding} \rightarrow Q_2 \rightarrow Q_4 \rightarrow L_r$

The current of L_r gradually decreases, and the energy accumulated in L_r also gradually decreases.

[Secondary Side] Q_5 , Q_8 , Q_6 , and Q_7 are On

On secondary side, in addition to Q_6 and Q_7 , Q_5 and Q_8 are also turned on. Therefore, current flows through following two paths; first is from the source to drain of $Q_6 \rightarrow n_2$ Winding \rightarrow source to drain of Q_7 , and second is from the drain to source of $Q_5 \rightarrow n_2$ Winding \rightarrow drain to source of Q_8 .

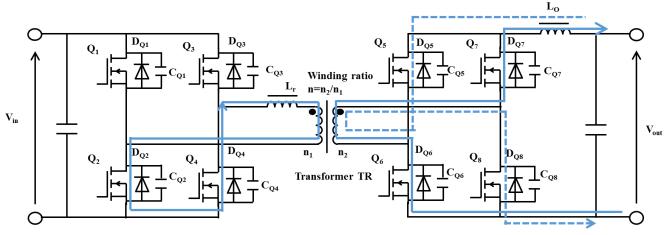


Fig. 3.12 Period g Operation

Period h-1 : C_{Q1}, C_{Q2} Charge/Discharge

[Primary Side] Only Q4 is On

Even after Q_2 turns off, current continues to flow through the following paths because of L_r energy:

 $L_r \rightarrow n_1 \text{ Winding} \rightarrow C_{Q2} \rightarrow Q_4 \rightarrow L_r$

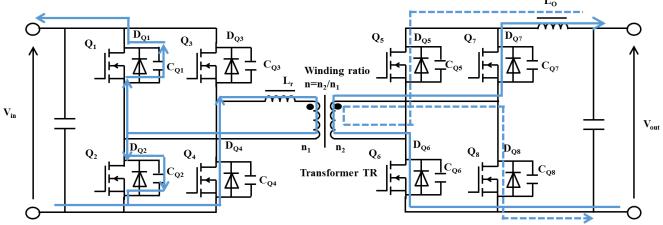
While C_{Q2} is getting charged, C_{Q1} is discharged in the following way:

 $L_r \rightarrow n_1 \text{ Winding} \rightarrow C_{Q1} \rightarrow V_{in} \rightarrow Q_4 \rightarrow L_r$

After C_{Q1} and C_{Q2} have been charged/discharged, the system moves to the next operation.

[Secondary Side] Q_5 , Q_8 , Q_6 , and Q_7 are On

Operation of period g continues.





Period h-2 : D_{Q1} Conduction

[Primary Side] Only Q₄ is On

The energy accumulated in L_r continues to flow through the following path even after C_{Q1} and C_{Q2} have been charged/discharged.

 $L_r \rightarrow n_1 \text{ Winding} \rightarrow D_{Q1} \rightarrow V_{in} \rightarrow Q_4 \rightarrow L_r$

In this condition, Q_1 turns on and the system moves to the next operation. Because D_{Q1} is conducting, Q_1 voltage is approximately 0 V and thus Q_1 turn on is ZVS.

[Secondary Side] Q₅, Q₈, Q₆, and Q₇ are On

Operation of period g continues.

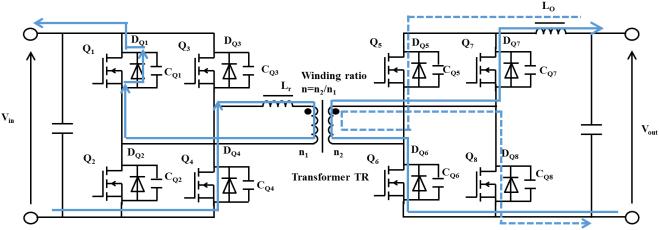


Fig. 3.14 Period h-2 Operation

Period h-3 : Q₁ Conduction

[Primary Side] Q_1 and Q_4 are On.

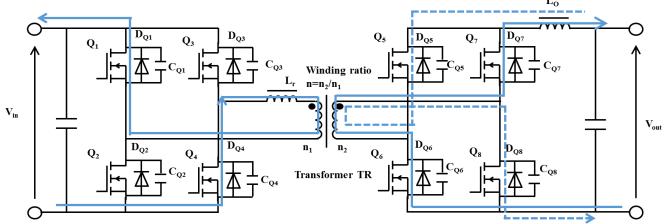
After Q_1 turns on, current continues to flow through the following paths because of L_r energy:

 $L_r \rightarrow n_1 \text{ Winding} \rightarrow Q_1 \rightarrow V_{in} \rightarrow Q_4 \rightarrow L_r$

In L_r , the incoming voltage V_{in} is applied in the direction that opposes this current flow, and thus the current of L_r is rapidly reduced, and is immediately inverted, and then the system moves to the next operation.

[Secondary Side] Q_5 , Q_8 , Q_6 , and Q_7 are On

Operation of period g continues.





3.2. Signal Waveform of Actual Operation

Fig. 3.16 shows operation waveforms of the primary side MOSFET Q_2 and Q_4 . Fig. 3.17 shows operation waveforms of the secondary side MOSFET Q_6 and Q_8 . Fig. 3.18 shows gate signal timing of each MOSFET.

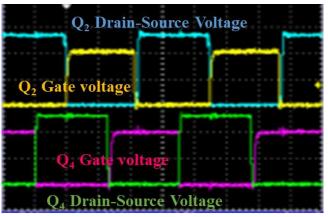


Fig. 3.16 Q₂, Q₄ Operation Waveforms

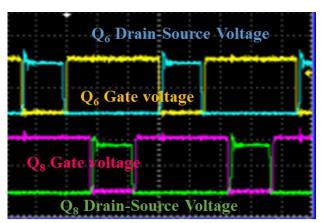
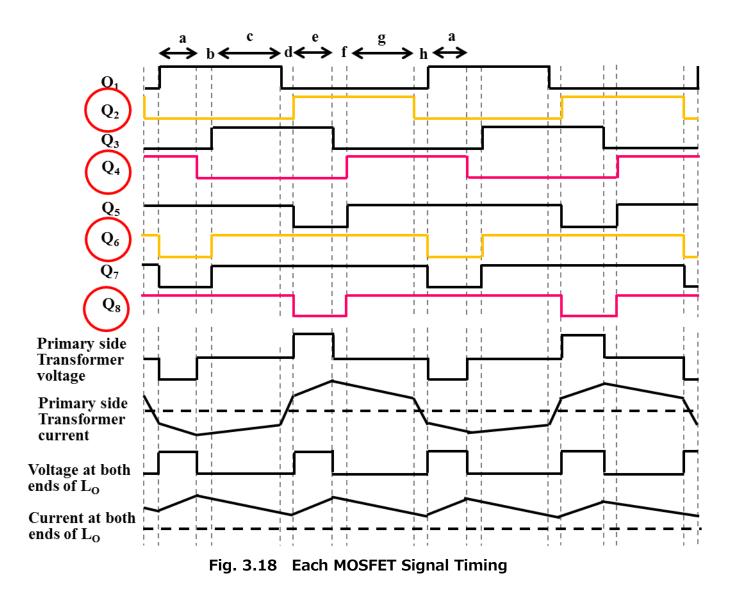


Fig. 3.17 Q₆, Q₈ Operation Waveforms



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